REMARKS

Claims 1, 5-6, 10, 12-15 and 21-23 are rejected under 35 U.S.C. § 102(a) as being unpatentable over Chen (US 5,648,793) in view of Moon (US 5,825,343) and further in view of Mano et al. (US 6,072,451), and claims 2-4, 7-9 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Moon and Mano et al. and further in view of Asada et al. (US 5,867,141). Applicant respectfully traverses these rejections on grounds that the applied references, whether taken singly or combined, fail to teach or suggest the combination of features recited by the amended independent claims 1, 5 and 10, and hence dependent claims 2-4, 6-9 and 11-14.

Independent claim 1 recites a method of driving a liquid crystal display panel of dot inversion system including, in part, "a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of a data driving integrated circuit; first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE); second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses," *(emphasis added).*

Similarly, independent claim 5, as amended, recites a driving apparatus for liquid crystal display panel of dot inversion including, in part, "a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data

output of the data driving integrated circuit; first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE); second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses."

Similarly, independent claim 10, as amended, recites a device for driving a liquid crystal display panel including, in part, "a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of the data driving integrated circuit; first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE); second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses."

In contrast to Applicant's claimed invention, Mano et al. explicitly teaches a flip-flop dividing a frequency of signal. Specifically, as reproduced below, Mano et al. explicitly discloses (at col. 28, lines 42-47):

> Another flip-flop 4701 further divides the frequency of the LC alternating clock 4012 inverted every frame, thereby to generate a signal 4709 which is

> inverted every second frame. Still another flip-flop 4702 further divides the frequency of the signal 4709 inverted every second frame, thereby to generate a signal 4710 which is inverted every fourth.

Accordingly, Applicants respectfully assert that Mano et al. explicitly teaches a flip-flop dividing a frequency of signal. Thus, Mano et al. is completely silent with regard to first and second delay means for delaying pre-gate start pulse. Therefore, Mano et al. fails to teach or suggest "a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of the data driving integrated circuit; first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE); second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses" as required by independent claims 1, 5 and 10.

For the above reasons, Applicant respectfully asserts that the rejections under 35 U.S.C. § 103(a) should be withdrawn because none of the applied prior art references, whether taken individually or in combination, teach or suggest the novel combination of features clearly recited in amended independent claims 1, 5 and 10, and hence dependent claims 2-4, 6-9 and 11-14, respectively.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and the timely allowance of the pending claims. Should the Examiner believe that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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